REMARKS

Reconsideration and allowance of this application, as amended, are respectfully requested.

Claims 1-3 stand rejected under 35 USC 103 as being unpatentable over Mitani (US Patent No. 6,018,185) in view of Omid-Zohoor et al (US Patent No. 5,777,370). This ground of rejection is respectfully traversed.

The structure of our claims 1-3 transistors is different from the structures taught by these two references. Specifically, the gate structure of our claim 1 transistor comprises a stacked structure of a gate oxide film, a first gate electrode and a second gate electrode, an oxide layer formed on a side wall of the first gate electrode, and nitride spacers formed on the oxide layer. The gate portion of Mitani in Fig. 2D comprises a stacked structure of a gate insulation film 106, a gate electrode 107, an upper gate-insulation film 108 and a side-wall gate insulation film 109. The gate portion of Mitani in Fig. 2I-Fig. 2L comprises a stacked structure of a gate insulation film 106, a gate electrode 107, a TiN barrier metal film 119, a tungsten wiring 120, and a side-wall gate insulation film 109. Mitani does not teach or even suggest a stacked structure of the first and the second gate electrodes, or the oxide film formed on the first electrode. Rather, it suggests a stacked structure of the gate electrode 107 and the upper gate-insulation film 108 or a stacked structure of the gate electrode 107 and the tungsten wiring 120 and the TiN barrier metal film 119 formed on a side wall and under the tungsten wiring 120. The oxide film and the TiN barrier film have different shapes and purposes. The purposes of TiN barrier film are to prevent the diffusion of impurities contained in the tungsten wiring into the gate electrode 119 and side-wall gate insulation film 109, and the oxidation of the tungsten wiring 119. However, the purpose of the oxide film is to reduce stress of the nitride spacers. Our claimed nitride spacers also differ from the side-

wall gate insulation film 109 because the nitride spacers of the present invention is disposed on the oxide layer which is formed on the side wall of first gate electrode while the side-wall gate insulation film 109 is formed on the side wall of entire gate portion. In addition, the second and third insulating films of Claim 1 only planarize the space above the active region and between the first gate electrode and the device isolation film while $NiSi_2$ film 111 and Si_3N_4 film 112 planarize the entire surface.

Thus, our claim 1 transistor significantly differs from Mitani. Likewise the combined teachings of Mitani and Omid-Zohoor do not suggest our claim 1 invention. Claims 2 and 3 depend from and further limit claim 1 and are therefore also allowable.

All outstanding matters having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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